CLAIMS

1. A method for forming a filled trench in a semiconductor layer of a semiconductor substrate, with the effect of trench voids minimised, the method comprising the steps of:

forming a trench in the semiconductor layer through a first face thereof, the trench defining an open mouth,

relieving the trench adjacent the open mouth thereof for preventing the commencement of bridging of the trench with a filling material at a level adjacent the first face of the semiconductor layer as the trench is being filled, and

filling the relieved trench through the open mouth with the filling material.

2. A method as claimed in Claim 1 in which the trench is sufficiently relieved for preventing commencement of bridging of the trench with the filling material at a level above a plane extending parallel to and below a plane to which the first face of the semiconductor layer is to be finished.

3. A method as claimed in Claim 1 in which the trench is relieved adjacent the open mouth thereof on one side of the trench.

4. A method as claimed in Claim 1 in which the trench is relieved adjacent the open mouth thereof on respective opposite sides of the trench.

5. A method as claimed in Claim 1 in which the trench is lined with at least one lining layer formed therein with a lining material prior to filling of the trench.

6. A method as claimed in Claim 5 in which the trench is relieved by relieving at least one of the lining layers adjacent the open mouth of the trench.

7. A method as claimed in Claim 5 in which the trench is relieved by relieving at least the lining layer first formed in the trench.

8. A method as claimed in Claim 5 in which the trench is relieved by relieving at

least one of the lining layers formed after the first of the lining layers to be formed.

9. A method as claimed in Claim 5 in which the trench is relieved prior to lining of the trench with the at least one lining layer.

10. A method as claimed in Claim 1 in which the trench is relieved to a depth from the open mouth in the range of 0.5μm to 5μm.

11. A method as claimed in Claim 1 in which each side of the trench which is relieved is relieved by tapering a portion of the side of the trench adjacent the open mouth, each tapered portion defining a tapering plane which converges towards the other side in a direction into the trench.

12. A method as claimed in Claim 11 in which the tapering plane defined by each tapered portion defines with a central plane bisecting the trench and extending longitudinally along the trench through the open mouth a relief angle in the range of 0.2° to 50°.

13. A method as claimed in Claim 12 in which the tapering plane defined by each tapered portion defines with the central plane a relief angle in the range of 4° to 40°.

14. A method as claimed in Claim 13 in which the tapering plane defined by each tapered portion defines with the central plane a relief angle in the range of 6° to 20°.

15. A method as claimed in Claim 12 in which each tapered portion defines at least two tapering planes defining respective different relief angles with the central plane.

16. A method as claimed in Claim 15 in which the tapering plane defined by each tapered portion which defines the greatest relief angle with the central plane is defined by the tapered portion adjacent the open mouth of the trench.

17. A method as claimed in Claim 16 in which the relief angles defined between the tapering plane of each tapered portion and the central plane decreases from the open mouth into the trench.

18. A method as claimed in Claim 1 in which each side of the trench which is relieved is relieved by forming a relieving recess into the first face of the semiconductor layer adjacent to and communicating with the trench adjacent the open mouth.

19. A method as claimed in Claim 18 in which the relieving recess is concave when viewed in a direction into the trench.

20. A method as claimed in Claim 1 in which each side of the trench which is relieved is relieved along the entire length of the trench.

21. A method as claimed in Claim 1 in which the trench is relieved by etching.

22. A method as claimed in Claim 21 in which the etching of the trench is carried out by an RIE etch.

23. A method as claimed in Claim 22 in which the parameters of the RIE etch are controlled for minimising the depth of scallops formed by the RIE etch.

24. A method as claimed in Claim 21 in which the forming of the trench and the relieving of the trench are carried out by the same etching process, and the parameters of the etching process are ramped during the etching process for relieving the trench.

25. A method as claimed in Claim 24 in which the parameters of the etching process are controlled for minimising the formation of footings at the base of the trench.

26. A method as claimed in Claim 5 in which the first face of the semiconductor layer adjacent the trench is lined with the lining material during lining of the trench with at least one of the lining layers.

27. A method as claimed in Claim 26 in which the filling material and the lining material above the first face of the semiconductor layer are thinned to a level just above the first face of the semiconductor layer.

28. A method as claimed in Claim 26 in which the filling material and the lining material above the first face of the semiconductor layer are removed to a level co-planar with the first face of the semiconductor layer.

29. A method as claimed in Claim 1 in which the filling material is selected from any one or more of the following materials:

polysilicon,
silicon nitride, and
oxide.

30. A method as claimed in Claim 1 in which the filling material is deposited by a chemical vapour deposition process.

31. A method as claimed in Claim 5 in which the lining material is selected from any one or more of the following materials:

oxide,
silicon nitride, and
polysilicon.

32. A method as claimed in Claim 5 in which at least one of the lining layers is a deposited layer.

33. A method as claimed in Claim 32 in which each deposited lining layer is deposited by a TEOS deposition process.

34. A method as claimed in Claim 32 in which each deposited lining layer is deposited by a high conformality deposition process.

35. A method as claimed in Claim 5 in which at least one of the lining layers is a grown layer.

36. A method as claimed in Claim 5 in which at least one of the lining layers is densified prior to filling of the trench with the filling material.

37. A method as claimed in Claim 1 in which the semiconductor layer is of silicon.

38. A method as claimed in Claim 1 in which the semiconductor layer is of single crystal silicon.

39. A method as claimed in Claim 1 in which the semiconductor substrate is a semiconductor layer of a semiconductor on insulator structure, and the filled trench extends to the insulating layer.

40. A method as claimed in Claim 39 in which the filled trench extends through the insulating layer.

41. A semiconductor substrate comprising a semiconductor layer, and a filled trench formed in the semiconductor layer, the filled trench being formed by the method as claimed in Claim 1.

42. A semiconductor substrate comprising:

a semiconductor layer having a first face, and

a filled trench extending into the semiconductor layer through the first face thereof, the trench defining an open mouth and having been relieved adjacent the open mouth prior to filling of the trench with a filling material for preventing the commencement of bridging of the trench with the filling material at a level adjacent

the first face of the semiconductor layer as the trench is being filled therewith.